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09/778,495	02/07/2001	Marquette John Anderson	TI-30831	8073

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EXAMINER	
LESNIEWSKI, VICTOR D	

ART UNIT	PAPER NUMBER
2155	5

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/778,495	Applicant(s) ANDERSON ET AL.	
	Examiner Victor Lesniewski	Art Unit 2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. Claims 1-20 are now pending.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file under Paper #2.

Information Disclosure Statement

4. The IDS filed on 4/2/2001 (Paper #3) has been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by DeRoo et al. (U.S. Patent Number 6,161,162), hereinafter referred to as DeRoo.

7. Some claims will be discussed together. Those claims which are essentially the same except that they set forth the claimed invention as a method are rejected under the same rationale applied to the described claim.

8. DeRoo has disclosed:

- <Claims 1 and 8>

  A processing device comprising: a master processor; a system memory; a slave processor subsystem including: a slave processor; a shared memory accessible by said master processor and said slave processor (column 2, lines 13-31); and an external memory interface allowing said slave processor to access said system memory (column 8, lines 21-30); and a verification interface for passing system memory accesses to said system memory in a normal mode and for passing said system memory accesses to said shared memory in a verification mode (column 81, line 50 through column 82, line 6).

- <Claims 4, 10, and 11>

  The processing device of claim 1 wherein said verification interface comprises multiplexing circuitry for passing data to said external memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode (column 82, lines 7-39).

- <Claim 5>

  The processing device of claim 4 and further comprising a control interface coupled between said master processor and said shared memory (column 2, lines 18-24).

- <Claim 6>

  The processing device of claim 5 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said external

memory interface responsive to whether said verification interface is in a normal mode or a verification mode (column 83, lines 28-44).

- <Claim 13>

  A processing device comprising: a master processor; a system memory; a slave processor subsystem including: one or more slave processors; a shared memory accessible by said master processor and said slave processor (column 2, lines 13-31); and a system memory interface allowing said slave processors to access said system memory (column 8, lines 21-30); and a verification interface for passing system memory accesses to said system memory in a normal mode and for passing said system memory accesses to said shared memory in a verification mode (column 81, line 50 through column 82, line 6).

- <Claim 14>

  The processing device of claim 13 wherein said system memory interface comprises: respective external memory interfaces associated with each slave processor; and a memory arbiter for arbiting between memory accesses generated by each of said external memory interfaces (column 2, lines 13-31).

- <Claim 17>

  The processing device of claim 13 wherein said verification interface comprises multiplexing circuitry for passing data to said system memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode (column 82, lines 7-39).

- <Claim 18>

  The processing device of claim 17 and further comprising a control interface coupled between said master processor and said shared memory (column 2, lines 18-24).

- <Claim 19>

  The processing device of claim 18 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said system memory interface responsive to whether said verification interface is in a normal mode or a verification mode (column 83, lines 28-44).

Since all the limitations of the invention set forth in claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 were disclosed by DeRoo, claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 are rejected.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2, 3, 7, 9, 12, 15, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo, as applied above, in view of Baxter et al. (U.S. Patent Number 5,887,146), hereinafter referred to as Baxter.

11. DeRoo disclosed a multiprocessing computer system providing multiplexed address and data paths from multiple CPUs to a single storage device. In an analogous art, Baxter disclosed a

system for improving the efficiency of operation in multiprocessor systems using a cache coherency protocol. See column 7, lines 15-25. It is evident that Baxter's system is based on a multiprocessing computer system such as that of DeRoo's invention.

12. Although DeRoo did not explicitly state that his system included a cache or a protocol translator, Baxter taught both a cache memory and the translation of protocols. Since the inventions encompass the same field of endeavor, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system provided by DeRoo by adding a cache and the ability to translate protocols as provided by Baxter. This would make sense because it would improve the efficiency of operation of the system.

13. Thereby, the combination of DeRoo and Baxter discloses:

- <Claim 2>

  The processing device of claim 1 wherein said slave processor subsystem further includes a cache memory coupled to said external memory controller and said slave processor (Baxter, column 4, line 67 through column 5, line 21).

- <Claims 3 and 9>

  The processing device of claim 1 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claims 7 and 12>

  The processing device of claim 6 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system

memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claim 15>

  The processing device of claim 13 wherein said slave processor subsystem further includes cache memories associated with each of said slave processors (Baxter, column 4, line 67 through column 5, line 21).

- <Claim 16>

  The processing device of claim 13 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claim 20>

  The processing device of claim 19 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

Since the combination of DeRoo and Baxter discloses all of the above limitations, claims 2, 3, 7, 9, 12, 15, 16, and 20 are rejected.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

- Hayashi et al. (U.S. Patent Number 5,649,184) disclosed a multiprocessor system including shared memory for storing objects of shared or local processing.
- Landi et al. (U.S. Patent Number 6,163,828) disclosed a multiprocessor system where two processors share a memory.
- Foster et al. (U.S. Patent Number 6,240,492) disclosed a memory interface for an integrated system which allows simultaneous access to multiple external memories coupled thereto.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Lesniewski whose telephone number is 703-308-6165. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hosain Alam can be reached on 703-308-6662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VL

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